Amendments to the Claims:

1 (Previously presented). A method of performing a Cyclic Redundancy Check (CRC) calculation, said CRC calculation done with N-bit at a time [500] over a binary string of data bits [520], said CRC calculation based on a generator polynomial G(X) [130] of degree d [131], said CRC calculation having intermediate and final results fitting a d-bit wide Field Check Sequence (FCS) [120], said generator polynomial allowing to form a multiplicative cyclic group comprised of d-bit wide binary vectors [400], said method comprising the steps of:

picking [1100] a new N-bit chunk of data bits from said binary string of data bits;

dividing [1110], modulo said generator polynomial G(X), said new N-bit chunk of data bits thus, getting a d-bit wide division result [535];

generating a value for FCS displaced within said cyclic group of d-bit wide binary vectors;

adding [1130], modulo two, said d-bit wide division result and said displaced d-bit wide FCS so generated;

updating [1140] said d-bit wide FCS;

checking if more data bits of said binary string of data bits are left for calculation:

if yes [1151], repeating all recited steps;

if not [1152], exiting the method after checking step;

thereby, getting a final result of said CRC calculation in said d-bit wide FCS.

2 (Previously presented). The method according to claim 1 wherein said final result is utilized to generate said d-bit wide FCS [510] for said binary string of data bits.

3 (Previously presented). The method according to claims 1 or 2 wherein said final result is a checking result of said binary string of data bits [520] including said d-bit wide FCS [510].

4 (Previously presented). The method according to claim 1 wherein said dividing step is omitted, if value of said N-bit is equal to said degree d.

5 (Previously presented). The method according to claim 4 wherein, if value of said N-bit is lower than said degree d, the further step of: padding said N-bit chunk of data with enough leading zeros to match said d-bit wide FCS [540].

6 (Previously presented). The method according to claim 1 wherein said CRC calculation is done from a most significant bit (MSB) [530] of said binary string of data bits and wherein said generating step includes a forward multiplication [560] of said d-bit wide FCS.

7 (Previously presented). The method according to claim 1 wherein said CRC calculation is done from a least significant bit (LSB) [710] of said binary string of data bits and wherein said generating step includes a backward multiplication [760] of said d-bit wide FCS.

8 (Previously presented). The method according to claim 1 wherein said binary string of data bits is a frame or message moved over a communications network.

9 (Previously presented). The method according to claim 1 wherein said binary string of data bits is derived or stored as a file in a computing system.

10. (Canceled)

11. (Canceled)

12 (Previously presented). A system, in particular a processor [1400], executing instructions for carrying out CRC calculations according to the method of claims 1 or 2.

13 (Previously presented). A system, in particular a state machine [1000] aimed at performing CRC calculations N-bit at a time, comprising means adapted for carrying out the method according to claims 1 or 2.

14. (Canceled)

15 (Previously presented). A computer-like readable medium comprising instructions for carrying out the methods according to claims 1 or 2.

16 (Previously presented). A method for calculating Cyclic Redundancy Check (CRC) including the acts of:

(a) selecting N-bits, N greater than 0, of data from a binary string of data bits;

(b) generating a value for FCS displaced within said cyclic group of d-bit wide binary vectors;

(c) adding (1130) modulo two, the N-bits and said value so generated; and

(d) updating said d-bit wide FCS.

17. The method of claim 16 further including the acts of:

(e) checking if more bits of said binary string are left for calculation;

(f) if yes, repeating acts (a) through (e);

(g) if not, existing with result in act (d) being the calculated CRC.

18 (Previously presented). The method of claims 16 or 17 further including the step of prior to performing step (b) dividing the N-bits, modulo generator polynomial G(x), to obtain a d-bit wide division result.

19 (Previously presented). The method of claim 1 wherein generating the value includes multiplying current FCS value by a displacement corresponding to the N-bit chuck of data bits.

20 (Canceled). A program product including:

a media in which computer program is recorded, said computer program including first instruction module for selecting N-bits, N greater than 0, of data from a binary string of data bits;

second instruction module generating a value for FCS displaced within said cyclic group of d-bit wide binary vectors;

third instruction module for adding module two, the N-bits and said value so generated; and

fourth instruction module, using results from third instruction module, to update said
d-bit wide FCS.